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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
GEBRESILASSIE, KIBROM K	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,319	ITO ET AL.	
	Examiner	Art Unit	
	Kibrom K. Gebresilassie	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9 and 11-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9 and 11-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/028319.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-9, and 11-17 have been presented for examination based on applicant's amendment filed on 30 August 2005.

2. Applicant has been canceled claims 2 and 10.

3. Claims 1, 3-9, 11-17 have been examined and rejected.

Response to Arguments

4. Applicants arguments filed on 07 September 2005 have been fully considered.

Regarding proposed drawing changes: Applicant's proposed drawing changes have been approved by the examiner pending review by the draftsperson.

Regarding objection of the specification: The examiner withdraws the objections to the specification in view of applicant's amendment to the specification filed on 30 August 2005.

Regarding applicant's response to 101 rejection: The examiner withdraws the 101 rejection in view of applicant's amendment to the claims arguments filed on 30 August 2005.

Regarding applicant's response to 103(a): Applicant's first argue that the prior art (Fakuda) does not teach displaying the influence of the boundary conditions on the inside of the calculation area. However, the examiner believed that the combination of the prior art of Fakuda and Hirotaka solve the argument of the applicant. Fakuda shows that the simulation data includes the boundary condition and displaying the influence of the boundary condition (Col. 14 lines 45-55). In addition, Hirotaka expressly teaches computing the area by supplying the boundary condition for a selected area within the whole area (Abstract), which clearly cure the limitation missed in the teaching of Fakuda.

Further, the applicant's argue that the invention made a user to recognize the boundary condition before the simulation. In response, the examiner notes the applicants have not specifically claimed recognize the boundary condition before the simulation in the language of the claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into claims.

Further, the applicant's argue that the prior art does not teach, "expanding the calculation area". In response, the examiner notes that in prior art by Kenichi teaches the limitation which recites " ... when the selected area is smaller than the whole, repeating procedure to select the next analysis area for the area with the error over the constant value again, and solving the whole ... (see page 1, Abstract)" is to be merely be interpreted as expanding the calculation area.

Regarding Amended claims 1,9, and 17: the amended limitations to include a "generating virtual image outside the calculation area according to the boundary condition; and displaying the virtual image, as well as real image included in the calculation area" are rendered obvious by the combination of Fukuda, and Hirotaka as now recited below under 103(a).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,099,574 issued to Fukuda in view of JP Publication No. 10125612 by Hirotaka.

As per amended claim 1:

Fukuda discloses a method of simulation for designing a semiconductor device with simulation data of the semiconductor device (Abstract), comprising:

determining whether or not the simulation data includes boundary conditions set for the simulation (col. 15 lines 27-32);

computing the influence of the boundary conditions if the simulation data include the boundary conditions (col. 15 lines 36-40);

displaying the influence of the boundary conditions (col. 14 lines 51-55)

prompting to enter an instruction whether or not the boundary conditions are changed (col. 15 lines 50-53); and

if an instruction to make no change in the boundary conditions is entered, carrying out the simulation with the simulation data (col. 15 lines 36-40).

Fukuda fails to disclose generating virtual images outside the calculation area according to the boundary condition; and displaying the virtual image, as well as real images included in the calculation area.

Hirotaka discloses generating virtual images outside the calculation area according to the boundary condition (page 4 [0006]); and displaying the virtual image, as well as real images included in the calculation area (page 4 [0006]; Fig. 2 and Fig. 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Fukuda related to semiconductor simulation required in designing and development of semiconductor devices with the teachings of Hirotaka related to a technique used in simulating the diffusion of impurity or point defects in a semiconductor manufacturing process. The motivation for doing so would have been more convenient to provide a simulation method capable of obtaining a highly accurate solution in a narrow

calculation region (page 5 [0008]). Hence a skilled artisan having access to the teaching of Fukuda and Hirotaka would have knowingly modified the teaching of Fukuda with Hirotaka.

As per claim 3:

Fukuda discloses after prompting to enter an instruction prompting to enter an instruction whether or not the boundary conditions used to generate the virtual images are adopted (col. 15 lines 50-53); and if an instruction to adopt the boundary conditions used to generate the virtual images is entered, carrying out the simulation by employing the adopted boundary conditions (col. 15 lines 36-40).

Fukuda fails to disclose if an instruction to make a change in the boundary conditions is entered, generating virtual images outside the calculation area according to boundary conditions other than the boundary conditions included in the simulation data; displaying the virtual images, as well as real images included in the calculation area.

Hirotaka discloses if an instruction to make a change in the boundary conditions is entered, generating virtual images outside the calculation area according to boundary conditions other than the boundary conditions included in the simulation data (page 10 [0023] lines 5-8); displaying the virtual images, as well as real images included in the calculation area (Fig. 2).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Fukuda related to semiconductor simulation required in designing and development of semiconductor devices with the teachings of Hirotaka related to a technique used in simulating the diffusion of impurity or point defects in a semiconductor manufacturing process. The motivation for doing so would have been more convenient to provide a simulation method capable of obtaining a highly accurate solution in a narrow calculation region (page 5 [0008]). Hence a skilled artisan having access to the teaching of Fukuda and Hirotaka would have knowingly modified the teaching of Fukuda with Hirotaka.

As per claim 4:

Hirotaka discloses computing and displaying the influence of other boundary conditions on the calculation area (page 4 [0006] lines 1-5).

As per claim 5:

Hirotaka discloses after prompting to enter an instruction: if an instruction to make a change in the boundary conditions is entered, expanding the calculation area and providing data concerning the expanded calculation area (page 10 [0025]).

As per claim 6:

Hirotaka discloses the boundary conditions include one of fixed, mirror, periodic, transmission, and infinite boundary conditions (reflection-type boundary condition;([0005] line 3).

As per claim 7:

Hirotaka discloses the boundary of the calculation area is changeable (page 10 [0025]).

As per claim 8:

Hirotaka discloses computing and displaying the influence of the boundary conditions includes: computing and displaying information about the accuracy and speed of the simulation to be carried out with the simulation data including the boundary conditions ([0004] lines 1-2, [0008]).

As per amended claim 9:

The limitation of claim 9 has already been discussed in the rejection of claim 1. It is therefore rejected under the same rationale.

As per amended claim 11:

The limitation of claim 11 has already been discussed in the rejection of claim 3. It is therefore rejected under the same rationale.

As per claim 12:

The limitation of claim 12 has already been discussed in the rejection of claim 4. It is therefore rejected under the same rationale.

As per claim 13:

The limitation of claim 13 has already been discussed in the rejection of claim 5. It is therefore rejected under the same rationale.

As per claim 14:

The limitation of claim 14 has already been discussed in the rejection of claim 6. It is therefore rejected under the same rationale.

As per claim 15:

The limitation of claim 15 has already been discussed in the rejection of claim 7. It is therefore rejected under the same rationale.

As per amended claim 16:

The limitation of claim 16 has already been discussed in the rejection of claim 8. It is therefore rejected under the same rationale.

As per amended claim 17:

Fukuda discloses a semiconductor device manufacturing method (semiconductor device fabrication processes; see Abstract, line 10), comprising:

designing a semiconductor device (col. 1 lines 9-11);

outputting design data of the semiconductor device (col. 1 lines 17-20);

simulating the design data of the semiconductor device employing a simulation data in connection with the semiconductor device (col. 15 lines 12-32), the simulating comprising:

determining whether or not the simulation data includes boundary conditions set for a boundary of a calculation area set for the simulation(col. 15 lines 27-32);

computing the influence of the boundary conditions on the inside of the calculation area if the simulation data includes the boundary conditions displaying the influence of the boundary conditions on the inside of the calculation area (col. 15 lines 36-40),

prompting to enter an instruction whether or not the boundary conditions are changed (col. 15 lines 50-53); and

if an instruction to make no change in the boundary conditions is entered, carrying out the simulation with the simulation data(col. 15 lines 36-40); and

fabricating the semiconductor device according to the design data (col. 15 lines 38-40)

Fukuda fails to disclose generating virtual images outside the calculation area according to the boundary condition; and displaying the virtual image, as well as real images included in the calculation area.

Hirotaka discloses generating virtual images outside the calculation area according to the boundary condition (page 4 [0006]); and displaying the virtual image, as well as real images included in the calculation area (page 4 [0006]; Fig. 2 and Fig. 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Fukuda related to semiconductor simulation required in designing and development of semiconductor devices with the teachings of Hirotaka related to a technique used in simulating the diffusion of impurity or point defects in a semiconductor manufacturing process. The motivation for doing so would have been more convenient to provide a simulation method capable of obtaining a highly accurate solution in a narrow calculation region (page 5 [0008]). Hence a skilled artisan having access to the teaching of Fukuda and Hirotaka would have knowingly modified the teaching of Fukuda with Hirotaka.

Conclusion

7. Applicant's amendment necessitated the new ground(s)**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

JP Publication No. 05-089212 issued to Kenichi et al.

U.S Patent No. 5,684,723 issued to Nakadai et al.

9. Any inquiring concerning this communication or earlier communication from the examiner should be directed to Kibrom K. Gebresilassie whose telephone number is (571) 272-8571. The examiner can normally be reached on Monday-Friday, 8:30 am to 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Kamini shah can be reached at (571) 272-2279. The official fax number is (571) 273-8300. Any inquiring of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is (571) 272-3700.

Kibrom K. Gebresilassie
Patent Examiner
U.S. Patent and Trademark Office
Simulation and Emulation, Art Unit 2128
401 Dulany St., Room 5C25 (Randolph)

KAMINI SHAH
PRIMARY EXAMINER

Alexandria, VA 22314-5774
Tel: 571-272-8571
Kibrom.gebresilassie@uspto.gov